II.1 Material Concepts

Materials differ in their ability to conduct electricity, which relates to their **electrical resistivity**, a measure of how strongly a material opposes the passage of electric current. Based on these properties, materials are classified into three main categories: conductors, semiconductors, and insulators, each with distinct resistivity values.

II.1.1Conductors

A **conductor** is a material that permits the flow of electric current when a voltage is applied across it. In solids, this flow occurs through free electrons. A typical conductor contains more than $\mathbf{10^{22}}$ free electrons per cubic centimeter, which enables efficient conduction. Its resistivity, denoted $\boldsymbol{\rho}$, characterizes the material's opposition to electric current, and is generally very low, typically below $\mathbf{10^{-8}\Omega.}\boldsymbol{m}$.

II.1.2 Insulators

On the opposite end, an **insulator** has very few free electrons, resulting in high resistivity, typically above $\mathbf{10^{6}\Omega.}\boldsymbol{m}$. This prevents the flow of electric current, making these materials ideal for applications requiring electrical insulation.

II.1.3 Semiconductors

Semiconductors are intermediate between conductors and insulators. At room temperature, they contain a small number of free electrons, but this number increases rapidly with temperature, causing a significant change in conductivity, which can range from $\mathbf{10^{-5}\Omega.}\boldsymbol{m}$ to $\mathbf{10\Omega.}\boldsymbol{m}$.

II.2 Energy Bands

Energy bands arise from the arrangement of electron energy levels in a material. In an isolated atom, electrons occupy distinct energy levels. However, when atoms come together to form a solid, their energy levels overlap, creating **energy bands**.

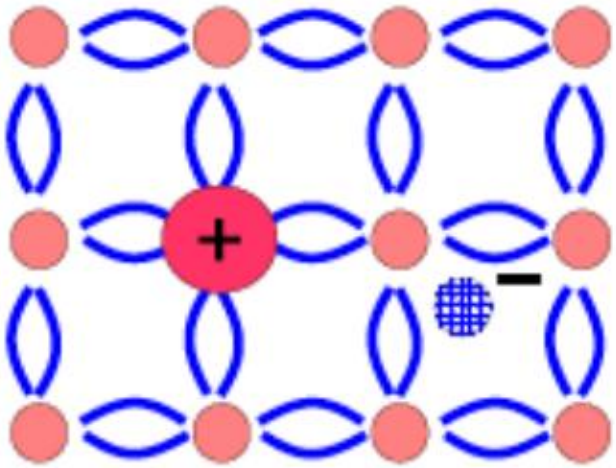
- **Valence and Conduction Bands**: In a solid, electrons primarily occupy two energy bands:
    - The **valence band** is the highest energy band occupied by electrons bound to atomic nuclei.
    - The **conduction band** lies above the valence band, where free electrons can move to conduct electricity.
- **Band Gap**: Between the valence and conduction bands is a gap or **forbidden band**. Its width determines the material's conductive properties:
    - In **conductors**, there is no band gap (the overlap is direct).
    - In **semiconductors**, the band gap is narrow, allowing electrons to cross the barrier under certain conditions.

- In **insulators**, the band gap is very wide, making it difficult for electrons to enter the conduction band.

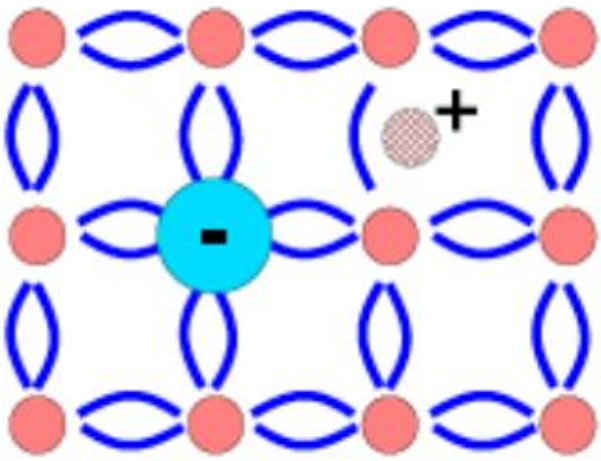
II.3 Semiconductors: Types and Characteristics

Semiconductors are especially interesting because their conductivity can be modified through processes such as doping.

- **Intrinsic Semiconductor**: An **intrinsic semiconductor** is a pure material with no added impurities. Its conductivity is low, relying solely on thermal agitation to allow some electrons to cross the band gap and enter the conduction band.
- **N-type Semiconductor**: **N-type (negative) doping** is achieved by adding impurities with excess electrons (such as phosphorus in silicon). This introduces additional free electrons to the material, thereby increasing its conductivity.



- **P-type Semiconductor**: **P-type (positive) doping** involves introducing impurities with fewer electrons, creating "holes" in the valence band (such as boron in silicon). These



holes allow neighboring electrons to move, thereby enhancing the material's conductivity.

II.4 Production of metallurgical-grade silicon (MG-Si):

The production of **metallurgical-grade silicon** (MG-Si) from quartz requires a multi-step chemical and thermal reduction process. Quartz (which is primarily silicon dioxide, SiO_2 is reduced using carbon at high temperatures to yield silicon. This process is carried out in an electric arc furnace and is energy-intensive due to the high temperatures needed to break down the SiO_2 structure.

a. Step-by-Step Process to Obtain Metallurgical-Grade Silicon from Quartz

1. **Preparation of Raw Materials**:
   - **Quartz**: The primary source of silicon, quartz, is cleaned and crushed to remove impurities.
   - **Carbon Source**: A carbon source, such as coke, charcoal, or coal, is used as the reducing agent. The quality and purity of the carbon source impact the final purity of the silicon.
2. **Reduction of Silicon Dioxide (Quartz) with Carbon**:
   - The quartz and carbon source are mixed in specific proportions (typically a ratio of about 2 parts SiO_2 to 3 parts carbon by weight).
   - This mixture is then fed into an **electric arc furnace**, where the temperature is raised to around 1700-2000°C.
   - At these high temperatures, carbon acts as a reducing agent, reacting with SiO_2 to produce silicon and carbon monoxide gas (CO).

b. Primary Reaction:

The main chemical reaction occurring in the furnace is as follows:

$SiO2+2C \rightarrow Si+2CO$

This endothermic reaction requires continuous energy input and occurs at high temperatures to overcome the stability of SiO2.

The molten silicon forms at the bottom of the furnace due to its higher density compared to the slag (impurities and unreacted carbon).

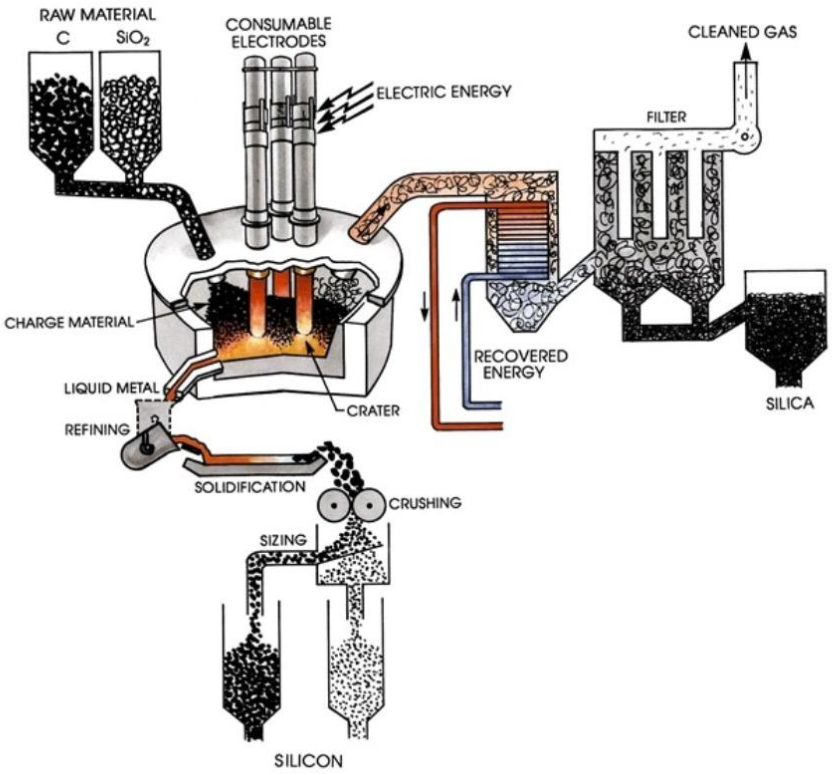


Figure 3: the different process steps to produce metallurgical grad silicon MG-Si

II.5 Purification of Metallurgical Grade Silicon

The purification of metallurgical grade silicon to obtain high-purity silicon, required in the electronics and photovoltaic industries, is a rigorous process comprising several chemical and thermal steps. Here are the detailed steps for achieving this purification:

Step 1: Conversion to Trichlorosilane

Metallurgical grade silicon (98-99% pure) is treated to remove metallic impurities through a chemical conversion process into trichlorosilane, a volatile molecule that allows for precise separation during distillation.

1. **Reaction with Hydrogen Chloride (HCl)**:
    - Silicon is heated to approximately 300°C and placed in a reactor where it reacts with gaseous hydrogen chloride (HCl).
    - This reaction generates trichlorosilane $SiHCl_3$ as well as hydrogen.

$$Si + 3HCl \rightarrow SiHCl_3 + H_2$$

The resulting trichlorosilane can be more easily purified through fractional distillation.

2. **Removal of By-products and Impurities**:
    - By-products such as dichlorosilane (SiH_2Cl_2 and tetrachlorosilane $SiCl_4$ may form. These by-products are separated during the distillation process.

Step 2: Fractional Distillation

Fractional distillation is used to further purify trichlorosilane. This method exploits differences in boiling points to isolate pure trichlorosilane from other contaminants.

1. **Heating and Separation of Compounds**:
    - The mixture of trichlorosilane is heated in a distillation column, where the trichlorosilane vaporizes at a lower boiling point than the impurities, allowing for separation.
2. **Isolation of Metallic Impurities**:
    - This step significantly reduces metallic impurities, as they remain in the non-volatile liquid residue.

Step 3: Thermal Decomposition and Chemical Vapor Deposition (CVD)

The purified trichlorosilane is then introduced into a chemical vapor deposition (CVD) reactor, where it is decomposed to obtain high-purity silicon.

1. **Thermal Decomposition**:
    - Trichlorosilane is heated to high temperatures, around 1000-1200°C, to induce its decomposition into silicon, releasing gaseous hydrogen chloride.

$$SiHCl_3 \rightarrow Si + Cl_2 + H_2$$

2. **Silicon Deposition**:
    - The silicon deposits in layers on heated filaments (often made of silicon), forming polycrystalline silicon with high purity.

Step 4: Cooling and Fragmentation

After deposition, the silicon is cooled and crystallized into bars or ingots, which are then crushed to form granules of purified silicon.

1. **Controlled Cooling**:
    - Controlled cooling promotes the formation of high-quality crystals without structural defects.
2. **Fragmentation**:
    - The silicon is then fragmented to facilitate transportation and subsequent processing steps.

Step 5: Purity Analysis and Quality Testing

The resulting silicon, known as electronic-grade silicon, is analyzed to ensure that its purity reaches a level of 99.9999% (6N), meeting industry standards for electronic applications.

1. **Spectrometric Analysis**:
    - Tests using mass spectrometry or ICP-MS (Inductively Coupled Plasma Mass Spectrometry) are employed to detect traces of metallic impurities.
2. **Crystallographic Control**:
    - Crystallographic analyses verify the quality of the crystal structure to confirm its suitability for electronic applications.

Summary

The purification of metallurgical grade silicon thus relies on a series of rigorous and precise steps:

- Conversion of metallurgical silicon to trichlorosilane for the isolation of metallic impurities.
- Purification by fractional distillation to obtain pure trichlorosilane.
- Thermal decomposition in a CVD reactor to deposit purified silicon.
- Cooling, fragmentation, and quality control of the purified silicon.

This process yields silicon suitable for the high demands of the electronics industry, ensuring optimal conductivity and low impurity levels for semiconductor applications and photovoltaic components.

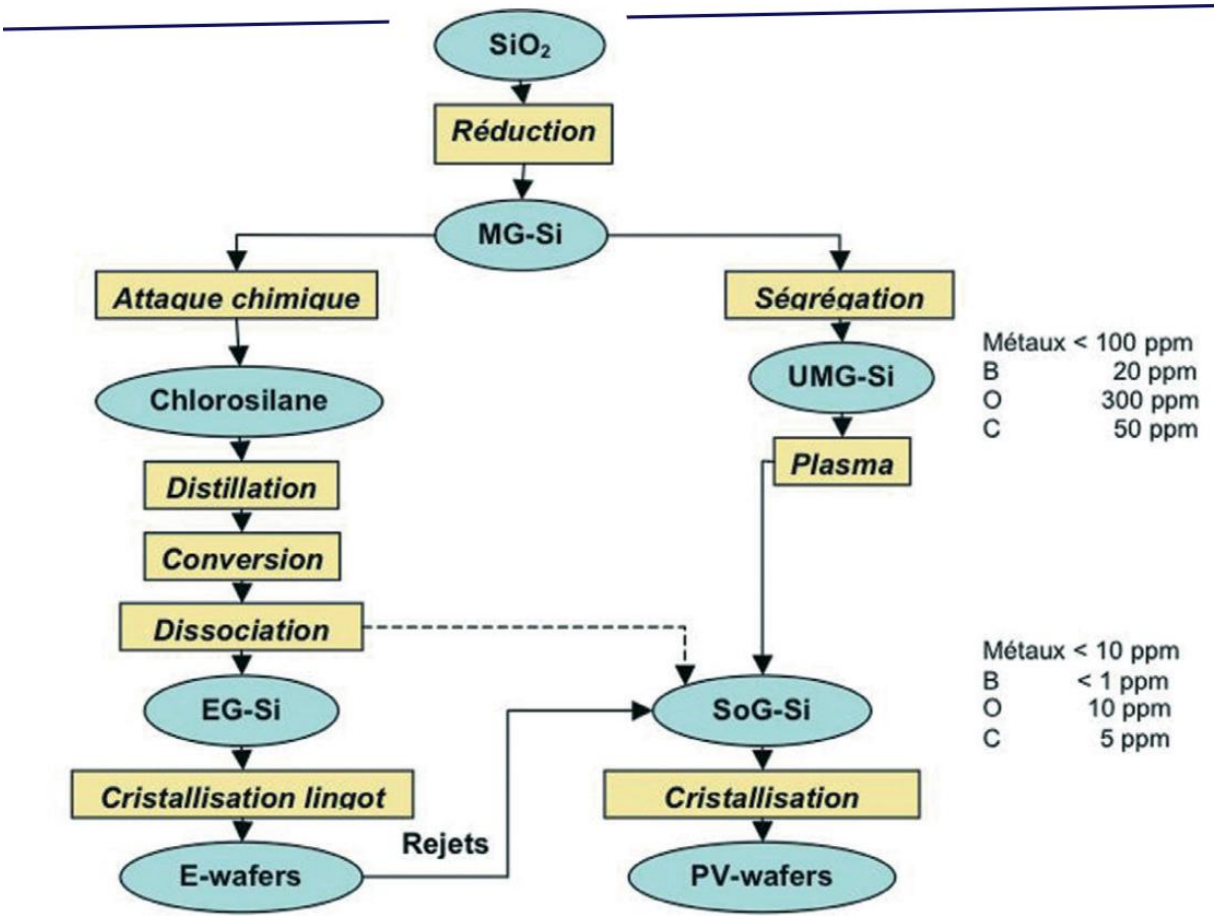


Figure 5 Comparison of supply chains. On the left, the classical route derived from electronic-grade silicon (EG-Si), and on the right, a direct route from upgraded metallurgical silicon (UMG-Si).
MG-Si: metallurgical-grade silicon, SoG-Si: photovoltaic solar-grade silicon, PV-wafers: photovoltaic wafers, E-wafers: electronic wafers.

II.6 Crystal Ingot Pulling and Growth

The growth of monocrystalline silicon ingots relies on sophisticated processes that yield high-purity crystals with a homogeneous structure. The two main methods for growing these crystals are the Czochralski (CZ) method and the Float-Zone (FZ) method. Each requires specific preparation steps, including the production of a seed crystal for the CZ method and an initial ingot for the FZ method.

II.6.1. The Czochralski Method (CZ)

a. Theory and Seed Crystal Preparation

The Czochralski method is based on the controlled crystallization of molten silicon, where a monocrystalline seed crystal is essential for initiating growth. This seed is a small fragment of

monocrystalline silicon, typically cut from a previously grown ingot. The seed crystal is carefully oriented according to the desired crystal structure for the final ingot, allowing control over the growth direction.

b. CZ Process Steps

1. **Silicon Melting**
   - Polycrystalline silicon is placed in a quartz crucible and melted in an inert atmosphere at around 1420°C, the melting point of silicon.
2. **Seed Crystal Introduction and Usage**
   - The monocrystalline silicon seed crystal is introduced into the silicon melt. To initiate monocrystalline growth, the seed is partially submerged and then slowly pulled. The seed's crystal structure dictates the alignment of the ingot's crystal lattice as it grows.
   - This initial immersion allows the molten silicon to solidify on the seed surface, adopting the seed's crystalline orientation.
3. **Pulling and Rotation**
   - The seed crystal is slowly pulled upward while rotating, allowing silicon atoms to crystallize in a monocrystalline structure. Precise control of the temperature and pulling speed (1-2 mm/min) maintains the ingot's diameter between 100 and 300 mm.
   - Simultaneous rotation of the crucible and seed ensures uniform thermal distribution, limiting growth defects and ensuring crystal uniformity.
4. **Ingot Solidification**
   - As the seed is pulled up, the molten silicon gradually crystallizes, adopting the monocrystalline structure. After the pulling process, the ingot is cooled and then sliced into wafers for electronic or photovoltaic applications.

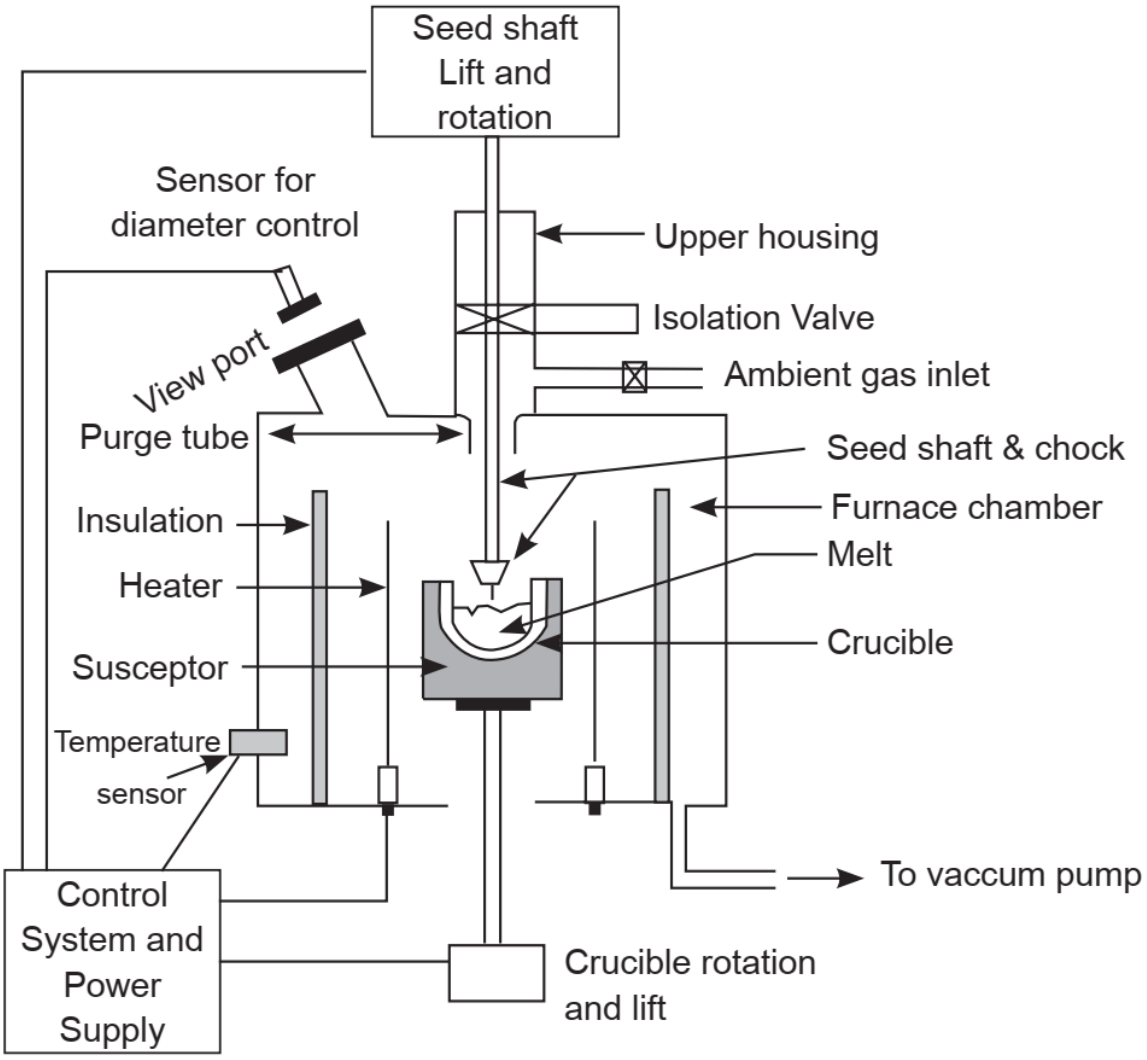


Figure 6 Czochralski crystal growth system

II.6.2. The Float-Zone Method (FZ)

a. Theory and Initial Ingot Preparation

The Float-Zone method is based on zone refining. This method is particularly suitable for achieving extremely high-purity silicon crystals, as it does not require a crucible, eliminating any potential contamination from quartz. However, the Float-Zone process requires an initial high-quality polycrystalline silicon ingot, which serves as the base for purification and monocrystal growth.

The initial ingot is made using refined polycrystalline silicon, which is compacted and processed into a solid polycrystalline structure. A small monocrystalline seed crystal is often attached to one end of the initial ingot to guide the monocrystalline structure during the Float-Zone process.

b. FZ Process Steps

1. **Preparation of the Polycrystalline Ingot**
   - A high-purity polycrystalline silicon ingot is produced using refined silicon. This polycrystalline ingot is positioned vertically, with a monocrystalline seed attached at one end to guide the crystal orientation.
2. **Creation of a Floating Zone**
   - An RF coil is used to create a localized melting zone in the ingot. This floating molten zone is maintained above the ingot without direct contact with a crucible, thus reducing contamination risks.
3. **Use of Seed Crystal for Monocrystalline Growth**
   - The monocrystalline seed crystal, attached to the end of the ingot, controls the crystal orientation of the solidifying zone as it moves. The molten zone is slowly moved along the ingot, allowing silicon atoms to align with the crystal structure of the seed upon solidification.
4. **Zone Refining for Purification**
   - As the molten zone advances along the ingot, impurities are driven toward the unmelted end of the ingot. These impurities are gradually concentrated in this end, which can be removed to produce a purified silicon ingot.
5. **Solidification and Monocrystal Formation**
   - The solidified ingot has a uniform monocrystalline structure with very high purity, thanks to the progressive elimination of impurities through the floating zone.

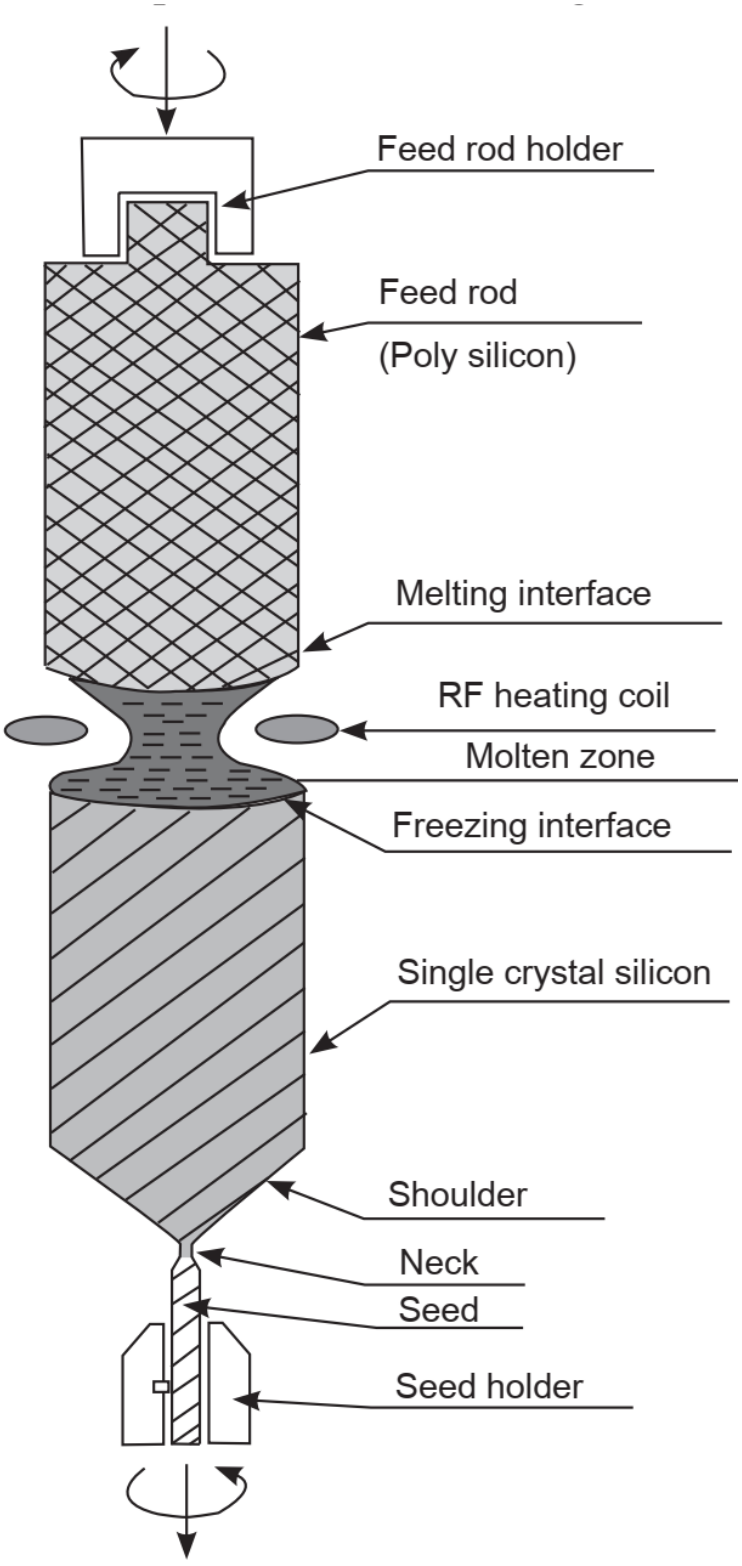


Figure7 Schematic diagram of Float zone process

II.6.3 Comparison of the two Methods

Feature	Czochralski (CZ) Method	Float-Zone (FZ) Method
Crystal Purity	High, though limited by possible contamination from the crucible	Extremely high, as it avoids crucible contact
Process Complexity	More complex due to the use of crucibles and temperature controls	Simplified due to the absence of crucibles
Diameter Control	Effective control over large-diameter ingots	Smaller diameter due to technical limitations
Application Areas	Widely used in semiconductor and photovoltaic industries	Primarily used in applications requiring ultra-high purity
Cost and Scalability	Lower cost, suitable for high-volume production	Higher cost due to precision and purity requirements

In conclusion, the CZ and FZ methods enable the production of monocrystalline silicon tailored to the specific needs of the electronics and photovoltaic industries. Mastering crystal growth, the use of seeds, and purification control are essential for producing high-quality crystals that meet the rigorous standards of modern devices.

II.7 Silicon Wafer Slicing

Slicing silicon ingots into thin wafers is a critical process in the manufacturing of semiconductor and photovoltaic devices. After producing a monocrystalline or polycrystalline silicon ingot, it must be sliced into wafers, requiring extreme precision to ensure uniform dimensions and minimize material loss, especially for high-quality wafers in electronics.

II.7.1. Slicing Techniques

Two main techniques are used to slice silicon wafers from ingots:

a. Diamond Wire Sawing

Diamond wire sawing is the most common method for slicing silicon ingots into wafers. A very thin, diamond-coated wire is wound around the ingot and acts as an abrasive cutting tool. The diamond particles on the wire grind away the silicon as it moves at high speed, allowing for controlled and precise slicing of the ingot into wafers.

- **Advantages**: This method offers high precision, enabling the production of ultra-thin wafers and minimizing material loss, an essential factor for cost-effective production in industries that use large silicon volumes.
- **Drawbacks**: Diamond wire sawing can be relatively slow and costly due to the wear on diamond-coated wires, which need regular replacement. Additionally, the technique

generates a significant amount of silicon dust, which requires efficient collection and disposal systems to avoid material waste and contamination.

Process Details: Diamond wire saws are typically composed of steel wire with diamond abrasives embedded in an adhesive coating. As the wire is tensioned around the ingot, it moves at high speeds to ensure a consistent abrasive action, cutting wafers with thicknesses that can range from 100 to 200 microns, depending on the requirements.

b. Laser Cutting

Laser cutting uses a high-energy laser beam to slice the silicon ingot into wafers. Though less common, it is ideal for applications that require extremely thin wafers or specialized geometries where traditional sawing methods may be less effective. The laser beam focuses heat to melt or vaporize the silicon along the desired cut line, creating clean, precise edges.

- **Advantages**: Laser cutting offers high cutting speed and exceptional precision, making it well-suited for thin wafers or complex wafer shapes. Additionally, it has minimal mechanical impact, reducing microcracks or fractures that can occur with mechanical sawing methods.
- **Drawbacks**: Laser cutting systems are more expensive and complex, making them a less economical choice for thicker wafers or applications that do not require ultra-thin slices. They also generate thermal stress, which may affect wafer quality if not carefully controlled.

Process Details: During laser cutting, the laser beam is directed onto the ingot's surface, with the beam intensity and pulse rate carefully controlled to achieve the desired cutting depth. The localized heat vaporizes or melts the silicon in a very narrow region, resulting in minimal material waste and smooth cut edges.

II.7.3 Edge Trimming

After slicing, the edges of the wafers are often irregular. Edge trimming is performed to remove these irregularities and ensure uniformity in the shape and dimensions of the wafers.

II.7.4. Thickness and Flatness Control

After slicing, each wafer undergoes strict thickness and flatness control checks. Uniform thickness is essential to ensure that each wafer has the same electrical properties and durability, which is critical in semiconductor applications. Flatness, or planarity, is also checked to ensure a smooth surface that will support the precise deposition of layers for electronic devices.

II.8. Cleaning and Preparation

Once sliced, wafers are carefully cleaned to remove silicon dust and other contaminants. They then undergo a chemical-mechanical polishing process to achieve an ultra-smooth surface, free from defects or impurities, making them ready for subsequent processing steps like doping and device fabrication. Her are the means steps of wafers cleaning

II.8.1. Initial Cleaning

This step is crucial immediately after slicing the silicon ingots into wafers. It aims to remove dust, debris, and other contaminants.

- **Ultrasonic Cleaning**
  - **Process**: The wafers are submerged in a cleaning solution, typically a mixture of deionized water and a mild detergent. An ultrasonic cleaner generates high-frequency sound waves, which create cavitation bubbles in the liquid. These bubbles collapse, generating shock waves that dislodge contaminants from the wafer surface.
  - **Duration**: This cleaning typically lasts between 5 to 15 minutes, depending on the level of contamination.
  - **Rinsing**: After ultrasonic cleaning, wafers are rinsed thoroughly with deionized water to remove any remaining cleaning solution.

II.8.2. Chemical Cleaning

Chemical cleaning is necessary to remove organic residues, metallic contaminants, and oxides that remain on the wafer surface after the initial cleaning.

- **RCA Clean Process**
  - **SC-1 Clean (Standard Clean 1)**
    - **Composition**: A mixture of hydrogen peroxide (H_2O_2), ammonium hydroxide (NH_4OH), and deionized water. Typical ratio: 1:1:5 (H_2O_2: NH_4OH: H_2O).
    - **Purpose**: This step removes organic contaminants, such as photoresist residues, and any particulate matter.
    - **Process**: The wafers are immersed in this solution at a temperature of approximately 70°C for about 10-20 minutes.
  - **SC-2 Clean (Standard Clean 2)**
    - **Composition**: A mixture of hydrogen peroxide (H_2O_2), hydrochloric acid (HCl), and deionized water. Typical ratio: 1:1:6 (H_2O_2: HCl: H_2O).
    - **Purpose**: This step removes metallic contaminants that may affect the electrical properties of the wafers.
    - **Process**: The wafers are immersed in this solution at approximately 70°C for another 10-20 minutes.

- **Final Rinsing**: After each cleaning step, wafers are thoroughly rinsed with deionized water to remove any residual chemicals.

II.8.3. Surface Preparation

After the chemical cleaning, further preparation ensures that the wafer surfaces are smooth and ready for the next fabrication steps.

- **Chemical-Mechanical Polishing (CMP)**
  - **Purpose**: CMP is used to achieve an ultra-smooth and uniform surface on the silicon wafers. This is crucial for ensuring good adhesion and uniform layer deposition in subsequent processes.
  - **Process**: Wafers are placed on a rotating polishing pad coated with a slurry containing fine abrasive particles (such as silica) and a chemical agent. The combination of mechanical abrasion and chemical etching removes surface irregularities.
  - **Duration**: The polishing process may last from several minutes to an hour, depending on the desired surface quality and wafer thickness.
- **Final Rinsing and Drying**
  - **Rinsing**: The wafers are rinsed thoroughly with deionized water to remove any polishing slurry or residual particles.
  - **Drying Methods**: Various techniques can be used:
    - **Nitrogen Blow Drying**: High-purity nitrogen is blown over the wafers to evaporate any remaining water droplets.
    - **Spin Drying**: Wafers are placed on a spinning platform that rapidly rotates to fling off excess water, allowing for a clean, dry surface.

II.8.4. Quality Control

After cleaning and preparation, wafers undergo stringent quality control checks to ensure they meet industry standards.

- **Visual Inspection**
  - Wafers are inspected under magnification for surface defects, contaminants, and any irregularities.
- **Thickness Measurement**
  - Using precision instruments, such as a micrometer or optical thickness gauge, wafers are measured for uniformity in thickness across each wafer and between wafers.
- **Electrical Testing**
  - Some wafers may undergo electrical tests (e.g., Hall effect measurements) to ensure that they meet the electrical specifications required for their intended applications.

II.8.5. Packaging and Storage

After successful cleaning and quality control checks, wafers are typically placed in cleanroom-compatible containers to avoid contamination. They are then stored in controlled environments until they are ready for use in further semiconductor fabrication processes.

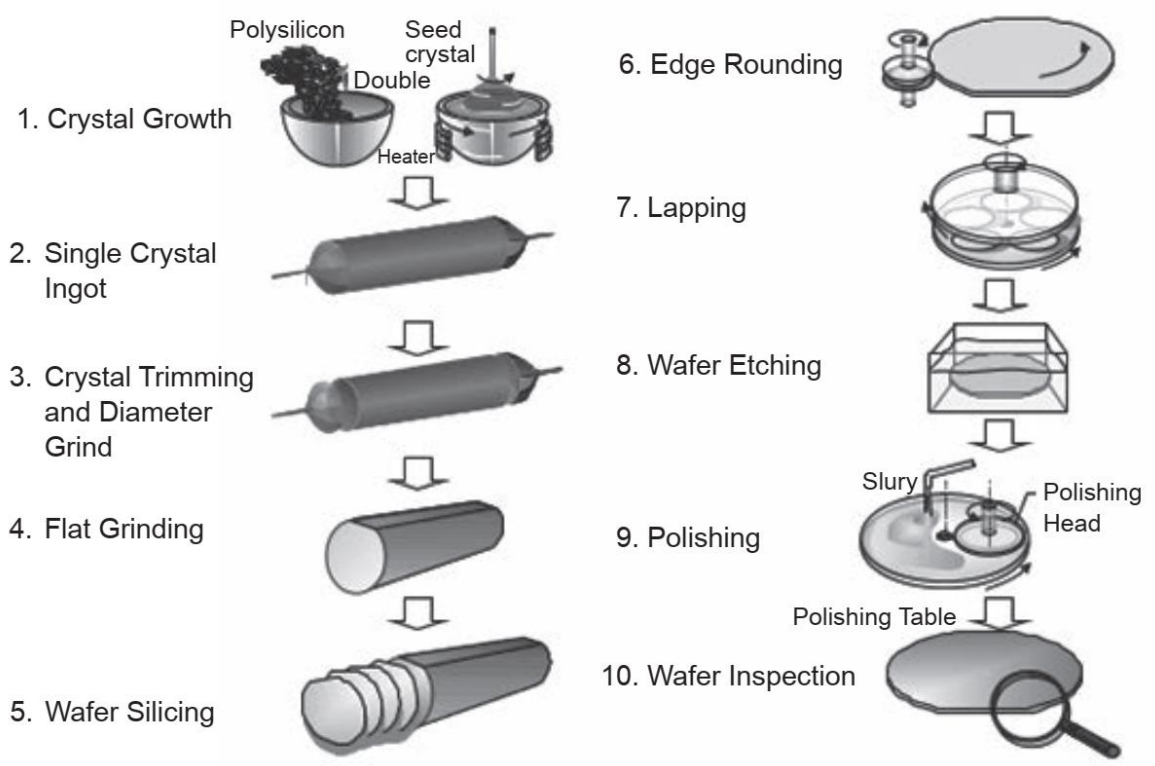


Figure 8 Process flowing steps of shaping of ingot to wafer