Concepts in Silicon Oxidation

Contents

1. Introduction to Oxidation
2. Types of Oxidation
3. Oxide Growth Model and Parameters
4. Oxide Furnaces and Processing Environments
5. Influence of Chlorine Additives on Oxidation
6. Effects of Crystal Orientation and Pressure on Oxide Growth
7. Impact of Impurities on Oxide Quality and Device Performance
8. Alternative Methods for Silicon Oxidation

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1. Introduction to Oxidation

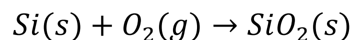
Oxidation refers to the conversion of a silicon wafer's surface into silicon oxide SiO_2 or SiO_x. This process is fundamental in semiconductor fabrication due to the protective and insulating properties of silicon dioxide, which provides electrical isolation and contamination resistance. Silicon's ability to form a stable oxide layer is a significant reason for its widespread use in semiconductor applications. This section introduces oxidation processes and highlights their role in integrated circuit (IC) fabrication, particularly in device isolation and surface passivation.

2. Types of Oxidation

In semiconductor fabrication, oxidation typically occurs through two main mechanisms: dry oxidation and wet oxidation.

Dry and wet oxidation need high temperature ($900 - 1200$°C) for growth, though the kinetics are different, which is why this process is called **thermal oxidation**.

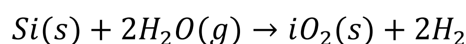
1. **Dry Oxidation** – In dry oxidation, silicon reacts directly with molecular oxygen (O_2) at high temperatures to form SiO_2. The reaction can be expressed as:



$$Si(s) + O_2(g) \rightarrow SiO_2(s)$$

   Dry oxidation produces high-quality oxide layers with minimal defects, making it suitable for applications requiring thin oxides.

2. **Wet Oxidation** – In wet oxidation, silicon reacts with water vapor (H_2O, resulting in a faster oxidation rate due to the enhanced reactivity of steam. The chemical reaction is:



$$Si(s) + 2H_2O(g) \rightarrow iO_2(s) + 2H_2$$

   This method is often preferred for thicker oxide layers, although it may introduce structural imperfections within the oxide.

3. Oxide Growth Model and Parameters

The Deal-Grove model is a widely used theoretical framework for describing the kinetics of silicon dioxide growth on silicon. This model divides oxide growth into an initial linear regime, dominated by surface reactions, and a subsequent parabolic regime where diffusion limits the growth.

The Deal-Grove Model

The oxide growth thickness ddd at time ttt is given by:

$$d^2 + A.d = B(t + \tau)$$

where:

- d is the oxide thickness,
- A is the linear rate constant (surface reaction-limited growth),
- B is the parabolic rate constant (diffusion-limited growth),
- τ represents an initial time offset, accounting for a native oxide layer.

Parameter Derivations

1. **Linear Rate Constant ($\boldsymbol{A}$)**
   The linear rate constant A depends on the reaction rate constant k_S and the gas-phase mass transfer coefficient hhh:

   $$A = \frac{2D}{k_S + h}$$

   where D is the diffusion coefficient of the oxidizing species in the oxide.

2. **Parabolic Rate Constant ($\boldsymbol{B}$)**
   The parabolic rate constant B is influenced by the diffusion of oxidizing species through the oxide and is given by:

   $$B = 2DC^*/N$$

   where:

   - C^* is the equilibrium concentration of oxidizing species in the oxide,
   - N is the moles of oxide formed per unit volume of silicon.
3. **Initial Time Offset ($\boldsymbol{\tau}$)**
   τ accounts for an initial oxide thickness d_i:

   $$\tau = \frac{(d_i^2 + A.d_i)}{B}$$

Under reaction-limited conditions (thin oxide layers), the growth rate follows a linear dependence on time:

$$d = \frac{B}{A}(t + \tau)$$

For thick oxides, where growth is diffusion-limited, the rate follows a parabolic law:

$$d^2 = Bt$$

These relationships enable predictions of oxide thickness over time, assuming equilibrium conditions.

4. Oxide Furnaces and Processing Environments

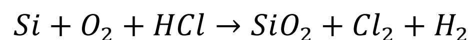
Thermal oxidation is typically performed in tube furnaces where silicon wafers are exposed to a high-temperature oxidizing atmosphere. Tube furnaces are divided into zones (source, center, load) to achieve uniform temperature and gas distribution. Vertical diffusion furnaces, commonly used for larger wafers, offer improved gas flow and temperature control, producing more uniform oxide layers. Both furnace types use filler wafers to help regulate gas flow and oxide uniformity across the wafer surface.

5. Influence of Chlorine Additives on Oxidation

Chlorine additives, such as hydrogen chloride (HCl) or trichloroethylene (C_2HCl_3), are introduced during oxidation to improve oxide quality and reduce mobile ions. Chlorine interacts with impurities in silicon dioxide, effectively reducing their mobility and trapping them in inactive states. This reduction in mobile ions, particularly sodium (Na^+), improves the oxide's electrical characteristics and reliability.

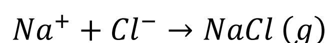
Chemical Reactions Involving Chlorine

1. **Chlorine and Silicon Dioxide Formation**
   Chlorine in the form of HCl participates in oxidation by interacting with impurities at the $SiO_2 - Si$-Si interface:

   $$Si + O_2 + HCl \rightarrow SiO_2 + Cl_2 + H_2$$

2. **Removal of Sodium Ions (Na^+)**
   Sodium impurities are a common contaminant in silicon processing. Chlorine binds with sodium ions to form volatile $NaCl$, which is expelled from the oxide:

   $$Na^+ + Cl^- \rightarrow NaCl\,(g)$$

   This process reduces charge traps and mobile ions at the oxide interface, enhancing device performance. Chlorine-based oxidation is especially beneficial for high-reliability applications where interface states and defect density must be minimized.

6. Effects of Crystal Orientation and Pressure on Oxide Growth

The crystallographic orientation of silicon affects oxidation rates due to differences in atomic density and surface reactivity. For instance, (100) silicon planes typically exhibit slower

oxidation rates than (111) planes, as the (100) orientation has a lower atomic density, resulting in fewer available silicon atoms at the interface.

Example: Sodium (Na) Impurities

In devices where Na impurities are present, differences in crystal orientation can impact impurity behavior. Sodium ions, which are highly mobile within the oxide, tend to accumulate differently on (100) and (111) surfaces due to variances in oxide density and defect sites associated with these orientations. On (100) planes, Na ions are less likely to migrate to the $SiO_2 - Si$ interface, whereas on (111) planes, they may accumulate, creating charge traps that degrade electrical properties.

Impact of Pressure

Higher pressures during oxidation increase the diffusion rate of oxidizing species, allowing for faster oxide growth. This adjustment enables more precise control over oxide thickness and uniformity. Pressure-enhanced oxidation is particularly useful for thick oxides, as it reduces oxidation time and helps maintain uniform layer properties.

7. Impact of Impurities on Oxide Quality and Device Performance

Dopants and impurities in silicon substrates significantly influence oxide growth and quality. Heavily doped n-type regions, for example, exhibit faster oxidation rates due to dopant-enhanced diffusion. Phosphorus, arsenic, or antimony dopants contribute to this accelerated growth, often resulting in non-uniform oxide layers. Dopant segregation at the $SiO_2 - Si$ interface can increase interface trap density, impacting device performance by shifting threshold voltages and reducing carrier mobility. For p-type dopants like boron, partial absorption into the oxide layer occurs, leading to depletion near the silicon surface. This section discusses impurity effects on oxide integrity and electrical characteristics, highlighting the importance of controlled doping for consistent device operation.

8. Alternative Methods for Silicon Oxidation

In addition to thermal oxidation, several alternative methods have been developed for silicon oxidation, each offering unique advantages for specific applications:

1. **Chemical Vapor Deposition (CVD)**
   In CVD, silicon dioxide is deposited onto the wafer surface by decomposing silicon and oxygen-containing precursors at high temperatures. Unlike thermal oxidation, CVD does not consume silicon, allowing oxide layers to be formed on various substrates without altering their dimensions. This technique is commonly used for interlayer dielectrics and planarization.
2. **Plasma-Enhanced Chemical Vapor Deposition (PECVD)**
   PECVD uses a plasma to activate precursor gases at lower temperatures than traditional CVD, enabling silicon dioxide deposition on temperature-sensitive devices. PECVD provides high deposition rates and good step coverage, making it ideal for complex device geometries.
3. **Low-Temperature Oxidation Using Nitric Acid**
   Ultra-thin oxides (20 nm or less) can be grown on silicon by exposing the surface to nitric acid at temperatures as low as 100 °C. This low-temperature process allows for

integration with conventional lithography steps without the thermal stress associated with high-temperature oxidation, making it suitable for applications requiring minimal thermal impact.

4. **Rapid Thermal Oxidation (RTO)**
   RTO uses high-temperature lamps to achieve rapid heating and cooling cycles, enabling controlled oxide growth in short time periods. This method is beneficial for producing thin oxides with minimal thermal diffusion, which is essential for advanced CMOS devices with stringent scaling requirements.

These alternative methods offer flexibility in oxide thickness, uniformity, and integration, enabling the precise tailoring of silicon oxide layers for specific device requirements.