VLSI Process Integration

10.1 INTRODUCTION

G. W. A. Dummar in 1952 recognized that electronic devices could be made from the single layers of conducting, insulating, amplifying and rectifying material. It was the first description in the integrated circuit development. The first circuit was germanium transistor, resistors and capacitors formed on a wafer. A modern VLSI fabrication development might be considered to have anywhere from 102 to 104 steps. Even transistors fabrication themselves is very complex as well, and varies drastically from process to process. Some examples of why fabrication step varies:

1. Will there be only a single type of PMOS transistor and a single type of NMOS transistor in the IC? Very unlikely in a complex modern design. If so, multiple lithography masks and multiple other steps may be necessary to independently pattern and dope the different types of devices.

2. Multigate devices like Graphene FET, G-MOSFET, FinFET might involve a more complex development to manufacture than traditional planar CMOS transistors.

3. In modern process technologies (e.g. 14-32 nm), the pitches of transistor gates, contacts, and other features are much less than the wavelength of light used to pattern them (typically 193 nm immersion lithography).

10.2 FUNDAMENTAL CONSIDERATIONS FOR IC PROCESSING

The process of constructing devices in a single piece of silicon crystal is a process of building successive layers of insulating, conducting and semiconducting material. Each layer is patterned to provide a distinct function and relationship with nearby areas and subsequent layers. The layers are manufactured and patterned by using the technique in the first 9 chapters of this book.

Building Individual Layers

Figure 10.1 shows some of the more important methods to create a layer in or on the silicon crystal. The layers are build by oxidation, implantation, deposition or epitaxial growth of silicon. Each of these layers can be created in two ways: 1. Uniform way 2. Selective way Uniformly formation is shown in left side of figure and selectively formation is shown in the right side of the figure.

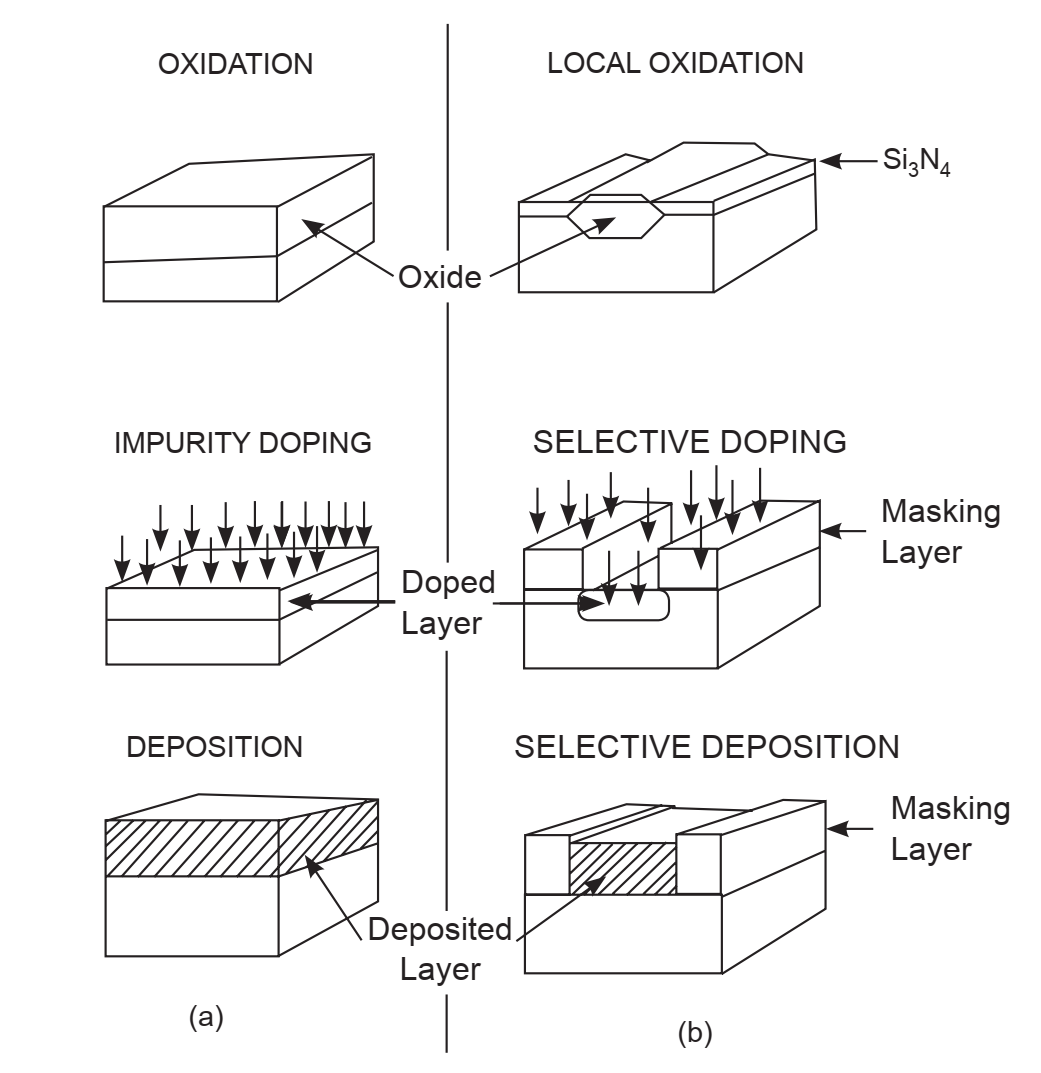


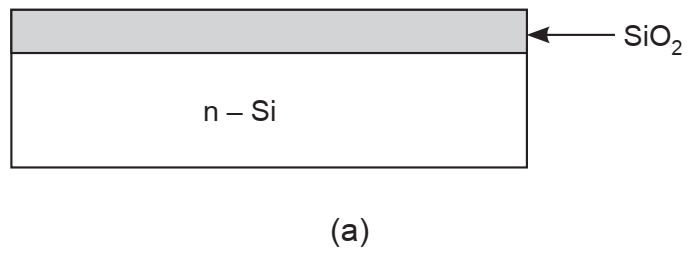
Fig. 10.1 Layers Formation in Silicon (a) uniform method (b) selective method

Photolithography and etching procedures are used to achieve patterning of the layers for selective formation. The various methods for obtaining individual layers have their own usefulness for specific applications. For example, if an insulating layer is required, the oxidation of silicon forms a layer of SiO2. However the formation of SiO2 layer consumes silicon and long thermal cycles for thicker layers. Therefore for a thick insulating oxide layer it might require an oxide deposition. The oxide deposited has a poor uniformity as compared to thermally grown oxide, but can be deposited at a lower temperature. At each step in process development, such analysis must be made to find which layer will give the desired results without affecting previous layers. Oxidation and deposition are the most common methods of forming a dielectric layer. The oxidation can be produced selective by depositing and patterning Si3N4 before oxidation. This technique is known as local oxidation.

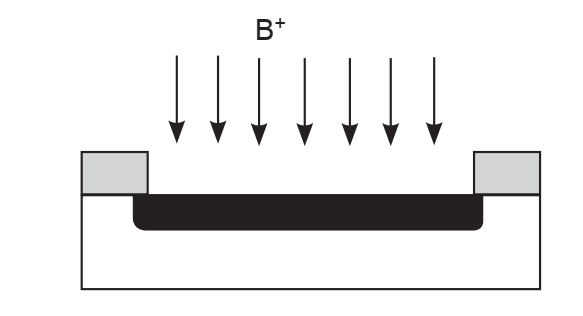
Integrating the Process Steps

In order to build layers requires careful consideration of each layer’s relative position to the others. Figure 10.2 shows example of this process of building layers. This schematic illustrates the sequence of forming a simple MOS capacitor.

Figure 10.2(a) shows initial oxidation formation. Then patterned process ia applied on oxide and etched to form the active region of the capacitor.



The active region is formed by ion implanting boron into the silicon exposed by the etching of the oxide as shown in figure 10.2(b).



The subsequent step of growing and patterning a thin oxide is shown in figure 10.2 (c) and figure 10.2 (d) shows depositing and patterning aluminum.

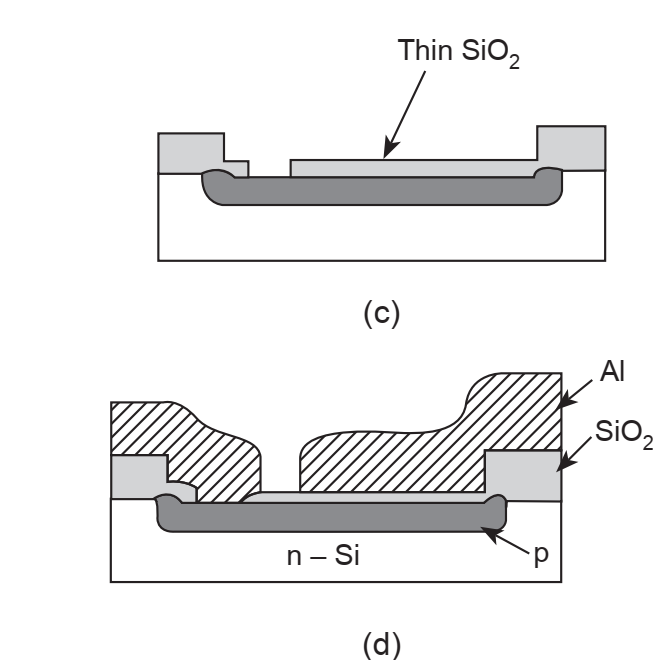


Fig. 10.2 Layers Integration

These steps describe consideration of integrating layers – alignment. The MOS capacitor that results from this process will only work properly if the individual layers are isolated except where an intentional contact is made.

Miniaturizing VLSI Circuits

The minimum feature size on each layer is determined by the ability to reproduce and resolve the feature routinely. This dimension is includes both the minimum dimension and how accurately that feature can be transferred into the silicon during the pattern transfer process. The pattern transfer process will affect the minimum feature size differently. The dry etching causes very little change in the dimensions of the feature etched in the patterned layer. The local oxidation causes the feature to grow as the oxide becomes thicker. Ion implantation involve lateral scattering, increasing the patterned feature size from the mask dimension. Dopants diffusion increases the feature size of a doped region of silicon. All these factors determine the final feature siae and must be taken into account when mask dimensions are determined.

10.3 NMOS IC TECHNOLOGY

There is a large diversity of basic fabrication steps used in the fabrication process of modern MOS Integrated circuits. The same fabrication process can be used for the designer of CMOS/BiCMOS devices. The commonly used base material is silicon-on-sapphire (SOS). To avoid the latch up problem i.e. presence of parasitic components like transistors, some variations are introduced in the techniques.

An nMOS process fabrication steps may be outlined as follows:

Step 1:

Processing is carried on single crystal silicon of high purity on which required P impurities are introduced as crystal is grown. Such wafers are about 75 to 150 mm in diameter and 0.4 mm thick and they are doped with say boron to impurity concentration of 1015/cm3 to 1016/cm3.

Step 2 :

A layer of SiO2 typically 1 μm thick is grown all over the surface of the wafer to protect the surface, acts as a barrier to the dopant during processing, and provide a generally insulating substrate on to which other layers may be deposited and patterned.

Step 3:

The surface is now covered with a layer of photo resist material. This is deposited onto the wafer and spun uniformly of the required thickness.

Step 4:

This photo resist layer deposited in above step is then exposed to ultraviolet light. For this mask are created. Mask defines regions through which diffusion process take place. Mask is divided into two area covered and open to ultraviolet light. The areas that are exposed to UV radiations become polymerized (hardened). While the areas where diffusion is required are shielded by the mask and remain unaffected.

Step 5:

Etching is next step in fabrication. Those areas which remains unaffected in previous step are etched away. The underlying SiO2 is also etched away to expose the wafer surface in the window defined by the mask.

Step 6:

Now a thin layer of SiO2 of 0.2 μm is deposited over entire surface again. Then poly silicon is grown on top of this oxide layer. This poly-silicon is deposited by CVD process. This forms gate structure. While fabricating pattern devices, accurate control of resistivity, thickness and impurity concentration is necessary.

Step 7:

Again photoresist coating is applied and mask is defined. Mask allow polysilicon to be patterned. After this n-type impurities are diffused through mask to define source and drain. Wafer is heated at very high temperature and passed through a chamber that contains desired n-type impurities. This is diffusion process.

Step 8:

Again a thick layer of SiO2 is deposited over entire surface. Then this layer is masked with photoresist. This is performed to define the area of source, gate and drain where connections (contact cuts) are to be made.

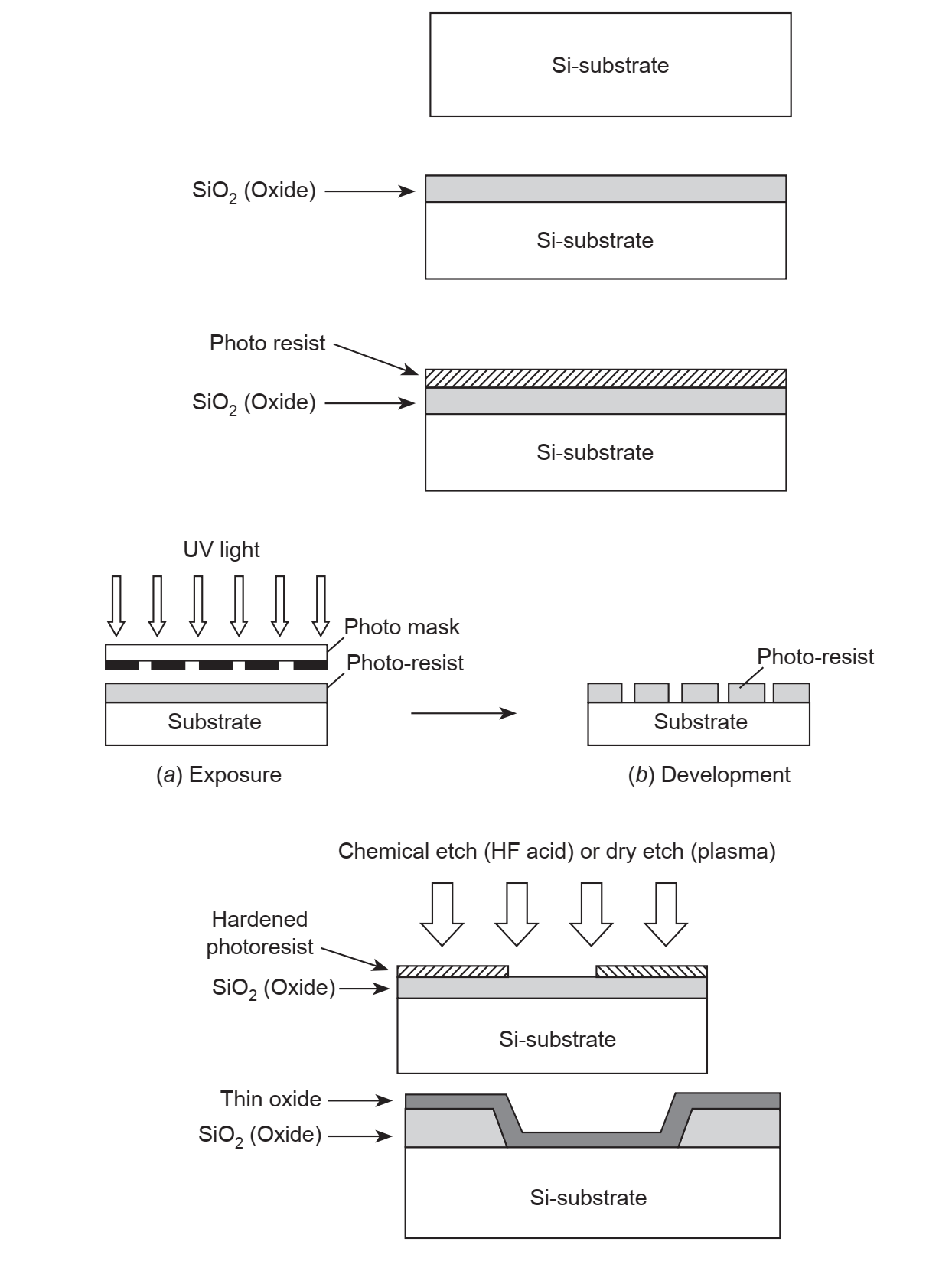
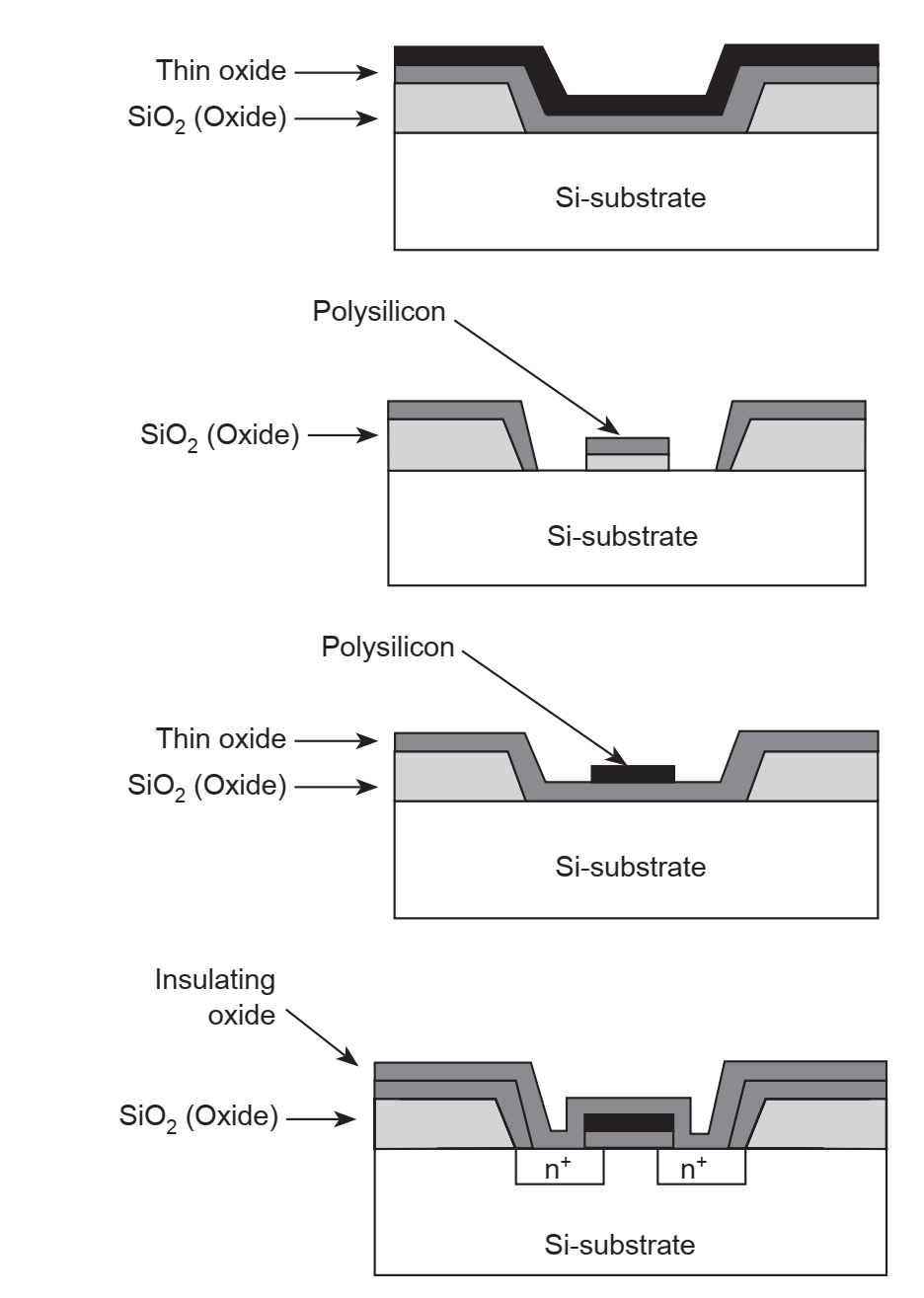


Fig. 10.3 NMOS Fabrication

Step 9:

Now metal generally aluminium is deposited over whole chip. Metal thickness is generally kept at 1 μm. then this aluminum layer is masked and etched to produce the interconnection pattern.

10.4 CMOS IC Technology

In early 1960’s Texas started the semiconductor manufacturing process and in 1963, Frank Wanlass got patent for CMOS technology. Since invention CMOS integrated circuits are fabricated by using the semiconductor device integrated fabrication process. These ICs are chief components of almost all electronic and electrical appliances in consumer segment. Most complex and simple electronic circuits are manufactured on a silicon wafer made of semiconductor compounds by utilizing different fabrication steps.

The CMOS technology is used in development of the processors, micro controllers, embedded systems, digital logic circuits and application specific integrated circuits. Its chief advantage is low-power dissipation, full logic swing, high-packing density and very low noise margin. Its most common application is in digital circuitry. The CMOS IC technology can be fabricated using three different processes. These are:

• N-well process

• P-well process

• Twin tub process

10.4.1 N-Well Process

The n-well fabrication steps are shown in figure 10.4. In the first step mask are used to defines well regions. Then diffusion process is utiliaed to form n-well at high temperature. Phosphorous implant is used for diffusion process. The depth of well is optimized so that there is no top diffusion breakdown.

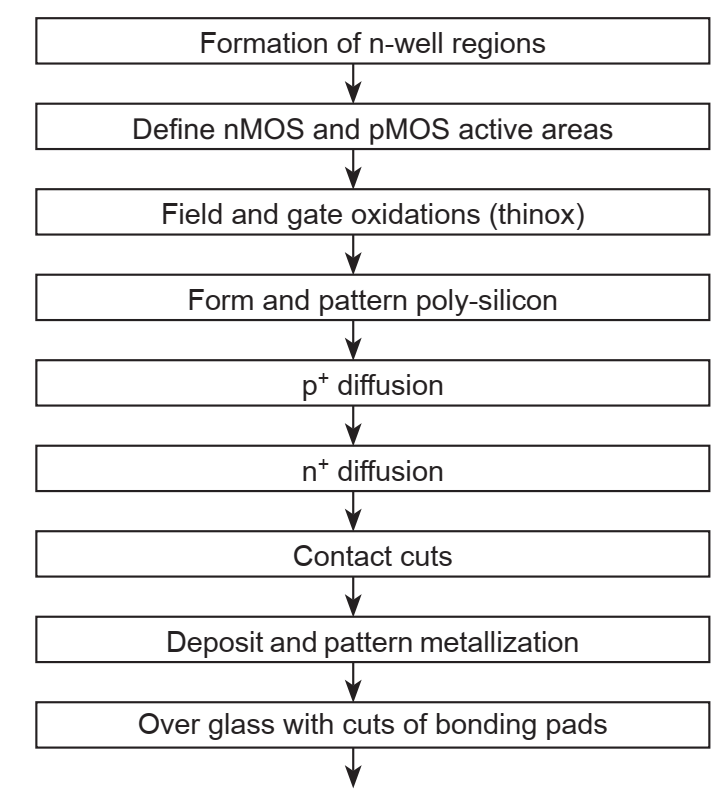
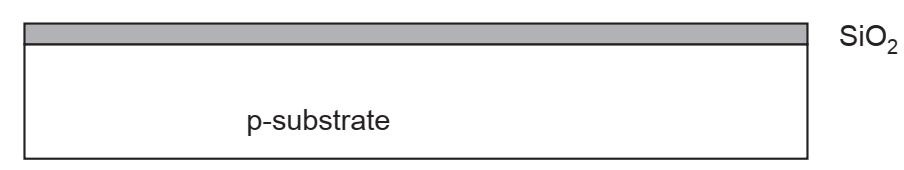


Fig. 10.4 N-well fabrication step

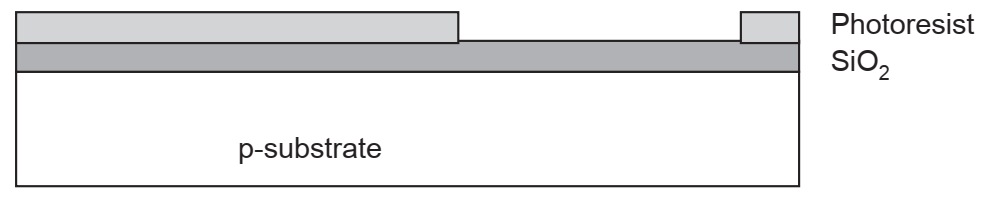
Then devices and diffusion paths are defined, field oxide is grown, polysilicon is deposit and patterned, diffusions process is carried out, contact cuts are made, and finally metallized. Figure 10.5 shows an CMOS inverter fabrication. In first step a blank wafer of Si is taken. This wafer is covered with a uniform layer of SiO2 using oxidation process.



Then the entire SiO 2 layer is covered with a layer of photoresist material. At this stage the material is highly insoluble. Now a mask is placed over substrate covered by SiO2 layer and then by photoresist material. Now it is exposed to UV light using the n-well mask. (Photolithography).

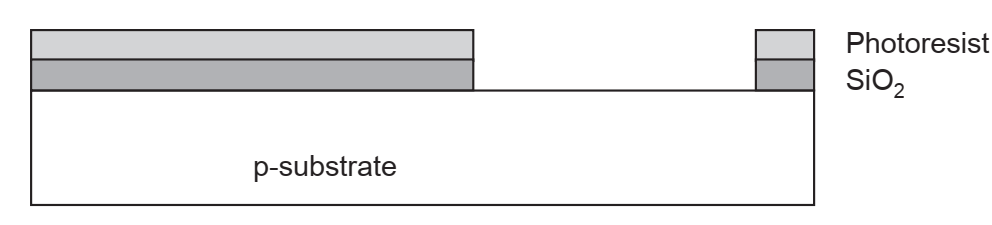


The area exposed to UV lights is removed using organic solvents. This is etching process in fabrication steps.

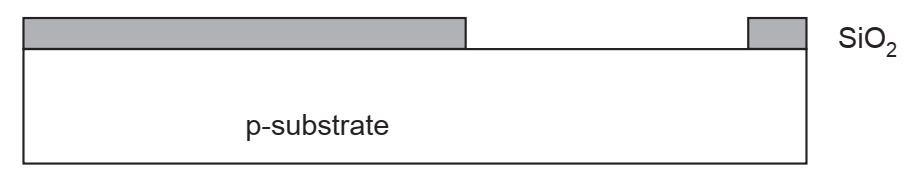


Next etching process is repeated to remove the uncovered oxide using Hydroflouric acid (HF).

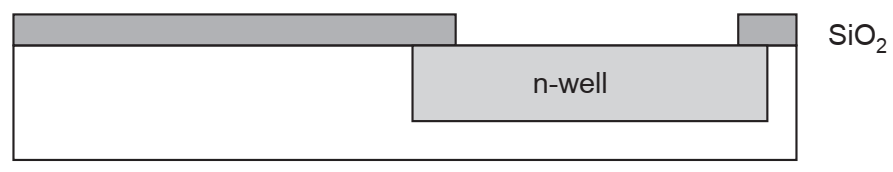
Using diffusion or ion implantation process, n-well is formed within p substrate.



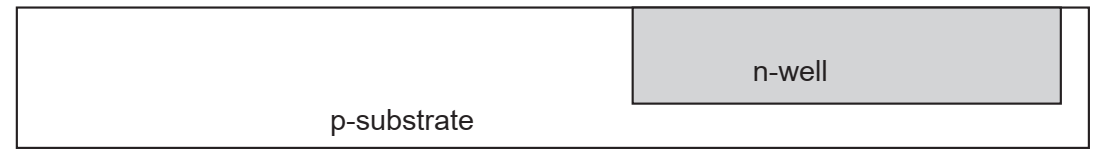
Then using acids remaining photoresist is etched away.



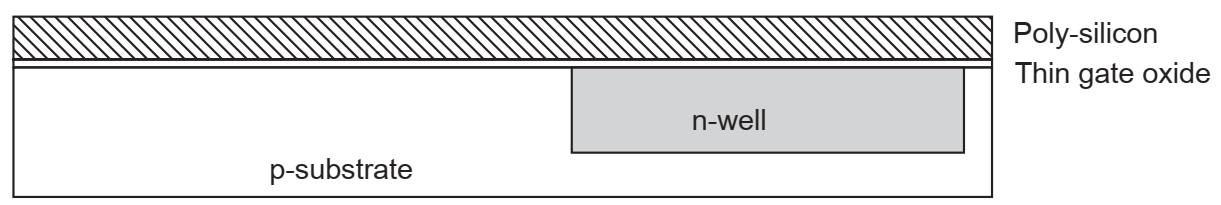
Using diffusion or ion implantation process, n-well is formed within p substrate.



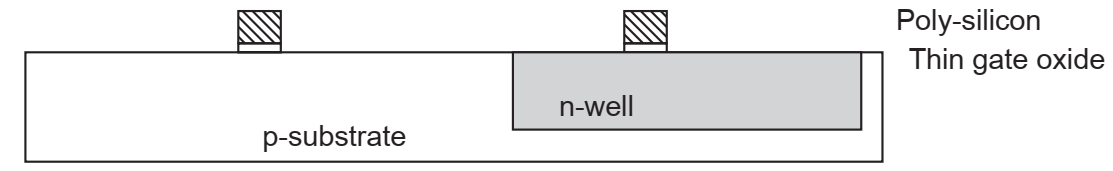
Again using HF acid remaining oxide is etched away. In subsequent steps photolithography process is repeated.



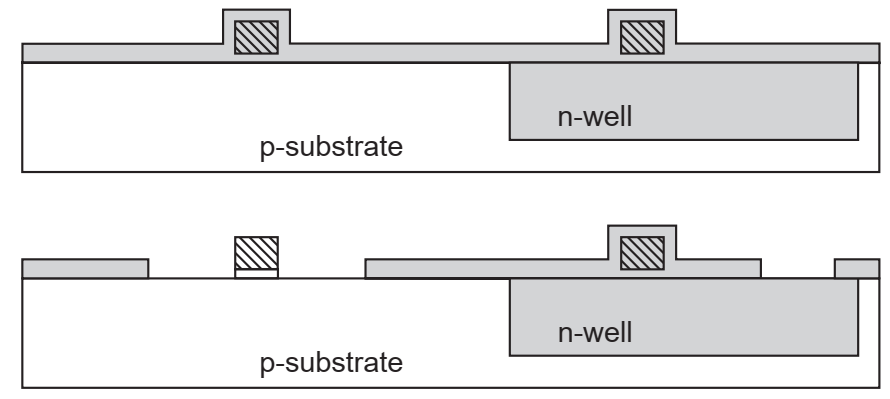
Deposit thin layer of oxide. Use CVD to form poly and dope heavily to increase conductivity



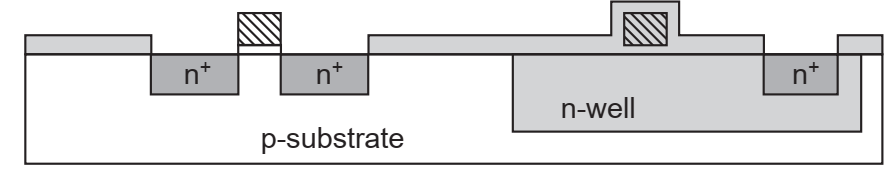
By photolithography process, pattern poly is applied.



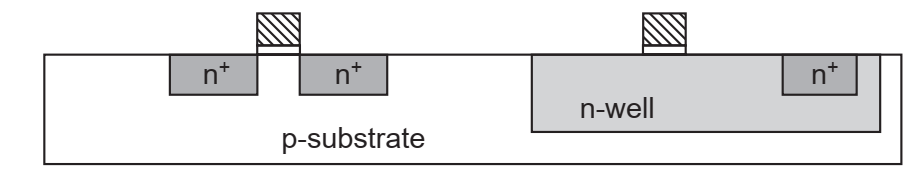
Then the entire surface is covered by a thin layer of oxide. This layer is deposited to produce n diffusion regions.



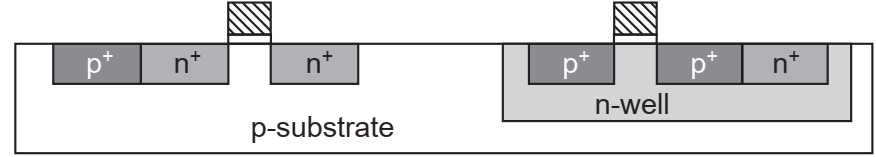
After this diffusion or ion implantation process is utilized to produce n diffusion regions



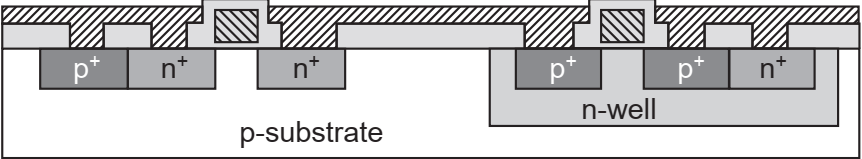
Using etching process the oxide layer is removed to complete patterning step.



Similar steps used to create p diffusion regions.



Remove excess metal leaving wires



**Fig. 10.5 N-Well process**